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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,396	08/28/2001	Hiroaki Yamoto	ADTST.031AUS	6154
7590	10/18/2004		EXAMINER	
MURAMATSU & ASSOCIATES Suite 225 7700 Irvine Center Drive Irvine, CA 92618			SIEK, VUTHE	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/941,396	YAMOTO ET AL.
	Examiner	Art Unit
	Vuthe Siek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 26 November 2001.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3,6,7,10-13,16 and 17 is/are rejected.
- 7) Claim(s) 4,5,8,9,14,15,18 and 19 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/26/01</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. This office action is in response to application 09/941,396 and Preliminary Amendment filed on 11/26/2001. Claims 1-19 remain pending in the application.

Drawings

2. Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 9 and 19 are objected to because of the following informalities: in step of "extracting...from data file...", "data file" should be changed to --a value change dump file-- in order to accurately describe the claim limitation according to the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-3, 6-7, 10-13 are 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over Rhim et al. (6,006,022) in view of Pieper et al. (5,371,851).

6. As to claims 1 and 10, Rhim et al. teach a method of validating design of complex integrated circuit (IC) under EDA systems (Figs. 1-17 and its description) comprising building prototype silicon based on IC design data produced under EDA systems (Fig. 1); applying event based test vectors derived from the IC design data to the prototype silicon by an event based test system and evaluating the response output to the prototype silicon (Fig. 1 and its description). Rhim et al. teach his invention accumulates processor events as programs and stored in circular buffers to be used by system designers for performance analysis. For example, if the microprocessor under development has a new design for interrupt service, this feature of the present invention can provide actual time data to verify whether the new interrupt service design in a fast manner (col. 12-13). These teachings would suggest one in circuit design validation, the circuit validation as taught by Rhim et al. would have included modifying the event based test vectors and feedbacking the modified event based test vectors to thereby correcting design errors in the IC design data. Accordingly, the claim invention of modifying and feedbacking steps would have been anticipated or obvious over Rhim's teachings. In addition, Pieper et al. a system to manipulate stimulus/response signal data associated with an IC design, where the system allows both design engineers and testers with ability of create stimulus vectors (event based test vectors) modify specific waveform events and state characteristics, prepare vector data for a specific tester, create a test program for a specific tester, simulate a tester's results through timesets and time generators, and resimulate a circuit design through translators to and from simulators (at least see Fig. 1, col. 8). Therefore, a combination teachings of Rhim and

Pieper or Rhim alone would have rendered the claim invention obvious to one of ordinary skill in the art at the time the invention was made because the modified event based test vectors would have reflected to silicon prototype test result, thereby design data stored in a design data base as in Rhim's Fig. 1 would be able to modify according that stored in the design data base to thereby can be used to produce a final silicon product.

7. As to claims 2, 3, 6-7, 11-13 and 16-17, Rhim et al. teach EDA systems include a simulator with event based test system through a software interface; extracting event format data through a testbench produced in the IC design data; creating a new testbench based on the modified event based test vectors from the events based test system. Pieper et al. teach means for waveform viewing editing waveform derived from the testbench created in the IC design data and means for changing clock rate and event timing data (at least see Fig. 1 and its description). The combination of teachings of Rhim and Pieper would have rendered the claim invention obvious to one of ordinary skill in the art at the time the invention was made because the EDA systems include viewer/editor would have provided design engineers and testers to interactively IC design where information of test results and IC design data can be shared, thereby this would speed up design process.

Allowable Subject Matter

8. Claim 9 and 19 would be allowed over the prior art of record after amending according to above suggestion the claim objection.

9. Claims 4-5, 8, 14-15 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER